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UNITED STATES PATENT APPLICATION

FOR

A CONTROLLED COLLAPSE CHIP CONNECTION (C4) INTEGRATED CIRCUIT PACKAGE WHICH HAS TWO DISSIMILAR UNDERFILL MATERIALS

INVENTORS: Suresh Ramalingam
Venkatesan Murali
Duane Cook

PREPARED BY:

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN
12400 Wilshire Blvd., 7th Floor
Los Angeles, CA 90025-1026
(714) 557-3800

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to an integrated circuit package.

2. BACKGROUND INFORMATION

Integrated circuits are typically assembled into a package that is soldered to a printed circuit board. Figure 1 shows a type of integrated circuit package that is commonly referred to as flip chip or C4 package. The integrated circuit 1 contains a number of solder bumps 2 that are soldered to a top surface of a substrate 3.

The substrate 3 is typically constructed from a composite material which has a coefficient of thermal expansion that is different than the coefficient of thermal expansion for the integrated circuit. Any variation in the temperature of the package may cause a resultant differential expansion between the integrated circuit 1 and the substrate 3. The differential expansion may induce stresses that can crack the solder bumps 2. The solder bumps 2 carry electrical current

between the integrated circuit 1 and the substrate 3 so that any crack in the bumps 2 may affect the operation of the circuit 1.

The package may include an underfill material 4 that is located between the integrated circuit 1 and the substrate 3. The underfill material 4 is typically an epoxy which strengthens the solder joint reliability and the thermo-mechanical moisture stability of the IC package.

The package may have hundreds of solder bumps 2 arranged in a two dimensional array across the bottom of the integrated circuit 1. The epoxy 4 is typically applied to the solder bump interface by dispensing a single line of uncured epoxy material along one side of the integrated circuit. The epoxy then flows between the solder bumps. The epoxy 4 must be dispensed in a manner that covers all of the solder bumps 2.

It is desirable to dispense the epoxy 4 at only one side of the integrated circuit to insure that air voids are not formed in the underfill. Air voids weaken the structural integrity of the integrated circuit/substrate interface. Additionally, the underfill material 4 must have good adhesion strength with both the substrate 3 and the integrated circuit 1 to prevent delamination during thermal and moisture

loading. The epoxy 4 must therefore be a material which is provided in a state that can flow under the entire integrated circuit/substrate interface while having good adhesion properties.

The substrate 3 is typically constructed from a ceramic material. Ceramic materials are relatively expensive to produce in mass quantities. It would therefore be desirable to provide an organic substrate for a C4 package. Organic substrates tend to absorb moisture which may be released during the underfill process. The release of moisture during the underfill process may create voids in the underfill material. Organic substrates also tend to have a higher coefficient of thermal expansion compared to ceramic substrates that may result in higher stresses in the die, underfill and solder bumps. The higher stresses in the epoxy may lead to cracks during thermal loading which propagate into the substrate and cause the package to fail by breaking metal traces. The higher stresses may also lead to die failure during thermal loading and increase the sensitivity to air and moisture voiding. The bumps may extrude into the voids during thermal loading, particularly for packages with a relatively high bump density. It would be desirable

to provide a C4 package that utilizes an organic substrate.

SUMMARY OF THE INVENTION

One embodiment of the present invention is an integrated circuit package which may include an integrated circuit that is mounted to a substrate. The package may further have a first underfill material and a second underfill material that are attached to the integrated circuit and the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a side view of an integrated circuit package of the prior art;

Figure 2 is a top view of an embodiment of an integrated circuit package of the present invention;

Figure 3 is an enlarged side view of the integrated circuit package;

Figure 4 is a schematic showing a process for assembling the integrated circuit package.

DETAILED DESCRIPTION OF THE INVENTION

Referring to the drawings more particularly by reference numbers, Figures 2 and 3 show an embodiment of an integrated circuit package 10 of the present invention. The package 10 may include a substrate 12 which has a first surface 14 and a second opposite surface 16. An integrated circuit 18 may be attached to the first surface 14 of the substrate 12 by a plurality of solder bumps 20. The solder bumps 20 may be arranged in a two-dimensional array across the integrated circuit 18. The solder bumps 20 may be attached to the integrated circuit 18 and to the substrate 12 with a process commonly referred to as controlled collapse chip connection (C4).

The solder bumps 20 may carry electrical current between the integrated circuit 18 and the substrate 12. In one embodiment the substrate 12 may include an organic dielectric material. The package 10 may include a plurality of solder balls 22 that are attached to the second surface 16 of the substrate 12. The solder balls 22 can be reflowed to attach the package 10 to a printed circuit board (not shown).

The substrate 12 may contain routing traces, power/ground planes, vias, etc. which electrically

connect the solder bumps 20 on the first surface 14 to the solder balls 22 on the second surface 16. The integrated circuit 18 may be encapsulated by an encapsulant (not shown). Additionally, the package 10 may incorporate a thermal element (not shown) such as a heat slug or a heat sink to remove heat generated by the integrated circuit 18.

The package 10 may include a first underfill material 24 that is attached to the integrated circuit 18 and the substrate 12. The package 10 may also include a second underfill material 26 which is attached to the substrate 12 and the integrated circuit 18. The second underfill material 26 may form a circumferential fillet that surrounds and seals the edges of the IC and the first underfill material 24. The sealing function of the second material 26 may inhibit moisture migration, cracking of the integrated circuit and cracking of the first underfill material.

The first underfill material 24 may be an epoxy produced by Shin-Itsu of Japan under the product designation Semicoat 5230-JP. The Semicoat 5230-JP material provides favorable flow and adhesion properties. The second underfill material 26 may be an anhydride epoxy produced by Shin-Itsu under the product designation Semicoat 122X. The Semicoat 122X material

has lower adhesion properties than the Semicoat 5230-JP material, but much better fracture/crack resistance.

Figure 4 shows a process for assembling the package 10. The substrate 12 may be initially baked in an oven 28 in step 1 to remove moisture from the substrate material. The substrate 12 is preferably baked at a temperature greater than the process temperatures of the remaining underfill process steps to insure that moisture is not released from the substrate 12 in the subsequent steps. By way of example, the substrate 12 may be baked at 163 degrees centigrade (°C).

After the baking process, the integrated circuit 18 may be mounted to the substrate 12. The integrated circuit 18 is typically mounted by reflowing the solder bumps 20.

The first underfill material 24 may be dispensed onto the substrate 12 along one side of the integrated circuit 18 at a first dispensing station 30. The first underfill material 24 may flow between the integrated circuit 18 and the substrate 12 under a wicking action. By way of example, the first underfill material 24 may be dispensed at a temperature between 110 to 120°C. There may be a series of dispensing steps to fully fill

the space between the integrated circuit 18 and the substrate 12.

The package 10 may be moved through an oven 32 to complete a flow out and partial gel of the first underfill material 24. By way of example, the underfill material 24 may be heated to a temperature of 120-145°C in the oven 32 to partially gel the underfill material 24. Partial gelling may reduce void formation and improve the adhesion between the integrated circuit 18 and the underfill material 24. The improvement in adhesion may decrease moisture migration and delamination between underfill material 24 and the IC 18 as well as delamination between underfill material 24 and the substrate.. The reduction in void formation may decrease the likelihood of bump extrusion during thermal loading. The package may be continuously moved through the oven 32 which heats the underfill material during the wicking process. Continuously moving the substrate 12 during the wicking process decreases the time required to underfill the integrated circuit and thus reduces the cost of producing the package. The substrate 12 can be moved between stations 30 and 34 and through the oven 32 on a conveyer (not shown).

The second underfill material 26 may be dispensed onto the substrate 12 along all four sides of the

integrated circuit 18 at a second dispensing station 34. The second material 26 may dispensed in a manner which creates a fillet that encloses and seals the first material 24. By way of example, the second underfill material 26 may be dispensed at a temperature of approximately 80 to 120°C.

The first 24 and second 26 underfill materials may be cured into a hardened state. The materials may be cured at a temperature of approximately 150 °C. After the underfill materials 24 and 26 are cured, solder balls 22 may be attached to the second surface 16 of the substrate 12.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific constructions and arrangements shown and described, since various other modifications may occur to those ordinarily skilled in the art.